SELF-CONTROLLED BINOMIAL COUNTERS

O. V. Ivanchuk – *Sumy State University, postgraduate student*
Galyna I. Lytvynenko – *English Language Adviser*

Counters take a special place among digital circuits used for data processing. Nowadays we more and more often face the task of improving their supervisory capacity. However, controlling their errors is a rather complex task, which requires the development of an additional control device added to the counter, the operation of which it is also necessary to check. Moreover, in this case the counter becomes an inhomogeneous structure, which is not easy to design and adjust while its reliability may even decrease.

One of the ways to overcome this contradiction is to use error-correcting number system, such as Fibonacci ones. The counters based on such a system are homogeneous and interference immune, since they do not contain special control devices, although equipment redundancy is still present in them like it is in binary counters. Binomial counters work similarly. One more important feature of binomial counters is significant reduction in the equipment required for decryption of their state, this in some cases leading to the reduction of hardware expenses as compared to similar devices implemented on the binary counters without error protection. In addition, these counters through changing the conversion factor and the control number k provide for changing the amount of noise and for adapting to the intensity and the nature of the noise, thus revealing a maximum of errors, which is not characteristic of Fibonacci counters. It is necessary to give a complete and profound analysis of binomial counters, as the available papers devoted to them focus mainly on the description of only one characteristic.

Let's consider the work of one of a number of well-known binomial counters described in [1]. It is of a binary type and is characterized by two main parameters – the numeral of bits n and control number k. It is described in [2].

The counter state number or the conversion index is determined by the number of unit combinations from (n+1) elements:

$$N = C_{n+1}^{k} = \frac{(n+1)!}{k!(n-k+1)!}.$$

Its states for k = 4 with the number of digits n = 5 in ascending order are shown in Table 1. Their number, obviously is $C_6^4 = 15$:

Table 1 – Counter states for k = 4 and n = 5

serial number	Digit 5 4 3 2 1	serial number	Digit 5 4 3 2 1	serial number	Digit 5 4 3 2 1	serial number	Digit 5 4 3 2 1
0	0 0 0 0 0	4	0 1 1 1 1	8	1 0 1 1 1	12	1 1 1 0 0
1	0 1 0 0 0	5	1 0 0 0 0	9	1 1 0 0 0	13	1 1 1 0 1
2	0 1 1 0 0	6	1 0 1 0 0	10	1 1 0 1 0	14	1 1 1 1 0
3	0 1 1 1 0	7	1 0 1 1 0	11	1 1 0 1 1		

If the counter by means of a single error or an error packet 0 → 1 comes to state 11111, i.e. it contains k + 1 units, it emits an error signal on the fifth output of the summator. The detecting ability of the counter to the errors 0 → 1 increases as the control number k decreases, while it reaches its maximum at k = 1. In this case the counter does not require any additional controlling devise, which means it is self-controlled and self diagnosed, this being one of the most important of its advantages.

LITERATURE

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